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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/897,902	07/05/2001	Isamu Hayashi	XA-9512	1411
181	7590	12/21/2005	EXAMINER	
MILES & STOCKBRIDGE PC 1751 PINNACLE DRIVE SUITE 500 MCLEAN, VA 22102-3833			LEE, CHRISTOPHER E	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 12/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 09/897,902	Applicant(s) HAYASHI ET AL.	
	Examiner Christopher E. Lee	Art Unit 2112	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08 December 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
 b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
 (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
 (b) ☐ They raise the issue of new matter (see NOTE below);
 (c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
 5. ☐ Applicant's reply has overcome the following rejection(s): _____.
 6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
 7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
 The status of the claim(s) is (or will be) as follows:
 Claim(s) allowed: _____.
 Claim(s) objected to: _____.
 Claim(s) rejected: 1, 2, 6 and 7.
 Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
 9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
 10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
See Continuation Sheet.
 12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). _____.
 13. ☐ Other: _____.

CEL/ 

Continuation of 11. does NOT place the application in condition for allowance because:

In response to the Applicants' argument with respect to "... Without concession as to the propriety of the outstanding rejection, the preamble of Independent Claim 1 has been amended to reinforce the structural relationship between the elements. It is well established that terminology in the preamble that limits the structure of the claimed invention is properly treated as a claim limitation." in the Response page 6, lines 1-9, the Examiner respectfully disagrees.

Actually, the recitation in the preamble, such that "a microprocessor on a semiconductor chip," has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. See *Kropa v. Robie*, 88 USPQ 478 (CCPA 1951).

In this case, the portion of the claim following the preamble "a microprocessor on a semiconductor chip" is a self-contained description of the structure not depending for completeness upon the introductory clause "a semiconductor chip" in the preamble, and so is the preamble denied the effect of a limitation where the claim is drawn to a structure. Thus, the Applicants' argument on this point is not persuasive.


In response to the Applicants' argument with respect to "... Applicants respectfully note that the rejection overlooks key deficiencies of Kakiage that undermine the asserted combination with Yanagiuchi. Kakiage teaches a processor 1 and two associated external devices 20 and 21. External device 20 operates asynchronously and does not receive a clock signal (see col. 7, lines 18-21). External device 21 operates synchronously and receives an external clock signal 100 (see col. 7, lines 23-24). Thus, Kakiage teaches only one external device that receives a clock signal and that device (device 21) is supplied by the external clock signal. The processor in Kakiage does not output a clock signal to either external device. ..." in the Response page 7, line 6 through page 8, line 16, the Examiner respectfully disagrees.

Even though Kakiage shows only 2 external devices in the exemplary embodiment, i.e., External device 20 and External device 21 in Fig. 1, Kakiage clearly discloses (1) the invention can be applied to a plurality of devices being connected to the External bus (See Kakiage, col. 17, lines 1-5), and (2) various other modification will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of the invention (See Kakiage, col. 17, lines 53-55). Therefore, Kakiage's invention could have a plurality of External devices 21 in synchronization with the External clock signal 100 in Fig. 1 because it would have been obvious to one having ordinary skill in the art at the time the invention was made to have connected said plurality of External synchronous devices to said External bus since it has been held that mere duplication of the essential working parts of said External synchronous device, which is connected to said External bus, involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Essentially, the Applicants argue that Kakiage teaches only one external device receiving a clock signal and that device being supplied by the external clock signal, and thus the processor in Kakiage does not output a clock signal to either external device. In contrary to the Applicants' argument, Kakiage impliedly teaches a plurality of External synchronous devices according to the above explanations, and the claimed features of bus control in Kakiage could be applied to said plurality of External synchronous devices as well as the exemplary embodiment's External devices 20, 21 in Fig. 1 in light of the Kakiage specification.

Furthermore, Yanagiuchi suggests that the first and second clock signals are output from the microprocessor to the first and second external devices, respectively, in parallel (See RCE Final Office Action mailed on 8th of September 2005, page 4, lines 16-23).

Therefore, the combination of Kakiage and Yanagiuchi with rationale teaches the obviousness of the claimed invention, and the Applicants' argument on this point is not persuasive.


REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/19/05